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ESE- 2018 (Prelims) - Offline Test Series

Test-1

ELECTRONICS & TELECOMMUNICATION ENGINEERING

SUBJECT: ANALOG ELECTRONICS, DIGITAL ELECTRONICS & MICROPROCESSORS – SOLUTIONS

01. Ans: (c)

Sol: The given circuit is a wein-bridge oscillator
The condition for sustained oscillations (or) the minimum voltage gain required to maintain the oscillations in a wein-Bridge oscillator is

$$A_V = 1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} \text{ ----- (1)} \quad [\text{where } R_1 =$$

$2R, R_2 = R, C_1 = C \text{ and } C_2 = 2C \text{ in the given circuit}]$

$$\Rightarrow 1 + \frac{R_f}{R_1} = 1 + \frac{2R}{R} + \frac{2C}{C} = 5 \text{ ----- (2)}$$

$$\Rightarrow R_f/R_1 = 4 \text{ ----- (3)}$$

$$\therefore R_f = 4R_1 \text{ -----(4)}$$

02. Ans: (c)

Sol: Step(1):

when $V_i = -2V, V_A = -12V$

Step (2):

$\therefore V_A = -12V, D \text{ is OFF} \Rightarrow V_0 = 0V$

03. Ans: (a)

Sol: Step (1) KVL for input loop

$$I_S = \frac{24V - 10V}{250\Omega} = 56mA$$

Step (2) KCL at (a)

$$I_L = I_S - I_Z$$

$$\text{Case (i): } I_{L_{\max}} = I_S - I_{Z_{\min}} = 53mA$$

$$I_{L_{\max}} = \frac{V_0}{R_{L_{\min}}} = 53mA$$

$$\therefore R_{L_{\min}} = \frac{10V}{53mA} = 188.679\Omega = 189\Omega$$

Case (ii):

$$I_{L_{\min}} = \frac{V_0}{R_{L_{\max}}} = I_S - I_{Z_{\max}}$$

$$= 56mA - 50mA = 6mA$$

$$\therefore R_{L_{\max}} = 10V / 6mA = 1.66k\Omega$$

04. Ans: (d)

Sol: Step (1): KCL at collector node of Q_1

$$I_{\text{Ref}} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1} + 2I_{B_2}$$

$$= I_{C_2} + \frac{2I_{C_2}}{\beta}$$

$$= I_{C_2} \left[1 + \frac{2}{\beta} \right]$$

$$\therefore \frac{I_{\text{Ref}}}{I_{C_2}} = \frac{I_{\text{Ref}}}{I_0} = 1 + \frac{2}{50} = 1.04$$



05. Ans: (d)

Sol: Given $A = 1000$ and $\beta = 0.0025$

$$20\% \text{ of } 1000 = 200$$

$$\Rightarrow A_{\text{New}} = 1000 - 200 = 800$$

$$\begin{aligned} \therefore A_{f_{\text{New}}} &= \frac{A_{\text{New}}}{1 + A_{\text{New}}\beta} \\ &= \frac{800}{1 + 800 \times 0.0025} \\ &= 266.667 \end{aligned}$$

06. Ans: (b)

Sol: Step (1):

$$\begin{aligned} f_{L_f} &= \frac{f_L}{1 + A\beta} \\ &= \frac{2\text{kHz}}{1 + 1000 \times 0.01} \\ &= 181.818\text{Hz} \end{aligned}$$

Step (2):

$$\begin{aligned} f_{H_f} &= f_H(1 + A\beta) \\ &= 20\text{kHz} \times (1 + 1000 \times 0.01) \\ &= 220\text{kHz} \end{aligned}$$

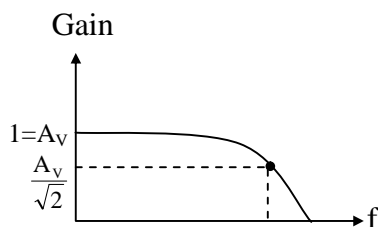
07. Ans: (b)

Sol: Bandwidth = $f_H = 1\text{MHz}$

At f_H , Gain of the amplifier, $A_v = \frac{1}{\sqrt{2}}$

$$\Rightarrow A_v = \frac{V_0}{V_i} = \frac{1}{\sqrt{2}} V$$

$$V_0 = \frac{V_i}{\sqrt{2}} = \frac{2}{\sqrt{2}} = \sqrt{2} V$$



08. Ans: (b)

Sol: In negative feedback amplifiers

Voltage gain ↓

Bandwidth ↑

Noise ↓

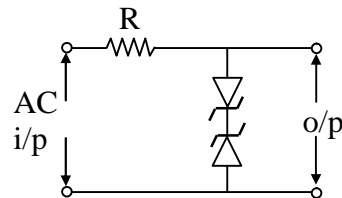
Distortion ↓

Amplitude fluctuations ↓

09. Ans: (a)

10. Ans: (d)

Sol:



11. Ans: (a)

$$\begin{aligned} \text{Sol: } V_H &= 2V_{\text{sat}} \left(\frac{R_2}{R_1 + R_2} \right) \\ &= 2 \times 10 \left(\frac{1}{1+9} \right) \\ &= 2V \end{aligned}$$

12. Ans: (c)

Sol: $V_0 = \text{gain} \times \text{input voltage}$
 $= A \times V_m \sin \omega t$ (i.e., $A \times V_m = V_x$)

$$\frac{dV_0}{dt} = V_x \cos \omega t \times \omega$$

$$SR = \left. \frac{dV_0}{dt} \right|_{\text{max}} = V_x 2\pi f$$

$$\Rightarrow 100 \times 10^6 = V_x \times 2\pi \times 20 \times 10^6$$

$$\begin{aligned} V_x &= \frac{100}{40\pi} \\ &= \frac{5}{2\pi} V \end{aligned}$$



13. Ans: (c)

Sol: $V_0 = -2(2) = -4V$

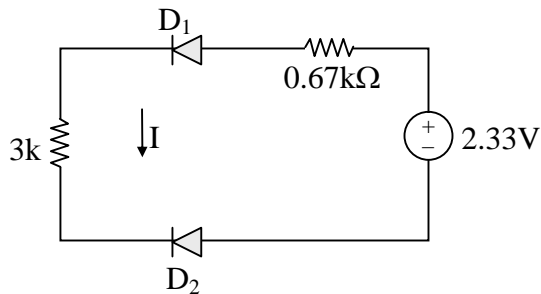
$$I_0 = -\frac{V_0}{2k} + \left(\frac{-V_0}{1k}\right)$$

$$= 2 \times 10^{-3} + 4 \times 10^{-3}$$

$$= 6mA$$

14. Ans: (a)

Sol: both the diodes are OFF
 $I=0$



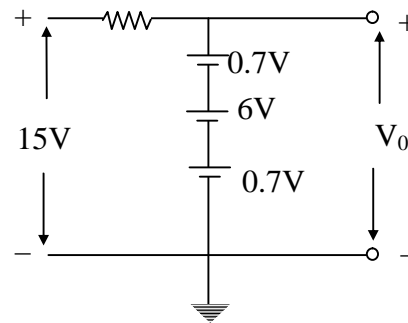
15. Ans: (c)

Sol: D → F B

Z_1 → operated in break down region

Z_2 → F B then

$$V_0 = 7.4V$$



Pre GATE-2018

COMPUTER BASED TEST

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16. Ans: (b)

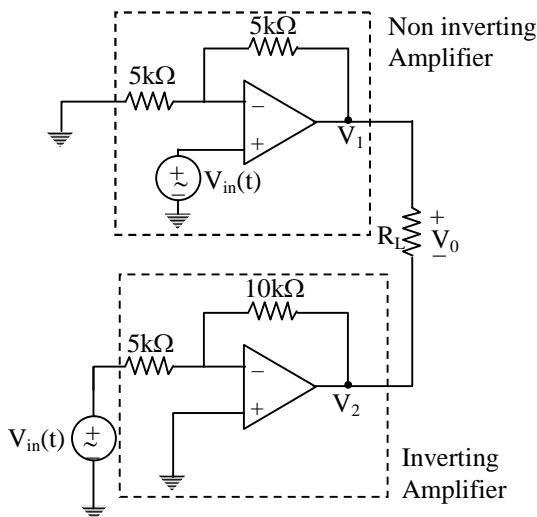
17. Ans: (d)

$$\text{Sol: } V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

$$\begin{aligned} V_1 - V_2 &= -2V \\ V_0 &= 5(-2) \\ &= -10V \end{aligned}$$

18. Ans: (d)

Sol: In Ideal op-amp $V_+ = V_-$ so equivalent circuit is



Output of the non-inverting amplifier is

$$\begin{aligned} V_1 &= \left(1 + \frac{5k}{5k}\right) V_{in}(t) \\ &= 2V_{in}(t) \end{aligned}$$

Output of the inverting amplifier is

$$\begin{aligned} V_2 &= \frac{-10k}{5k} V_{in}(t) \\ &= -2V_{in}(t) \end{aligned}$$

Therefore, the output voltage is

$$\begin{aligned} V_0 &= V_1 - V_2 \\ &= 2V_{in}(t) - (-2V_{in}(t)) \\ &= 4V_{in}(t) \\ &= 4 \times 3\sin\omega t \\ &= 12\sin\omega t \end{aligned}$$

19. Ans: (a)

Sol: For negative feedback, gain factor is reduces by $(1+A\beta)$ for shunt-series, R_{in} is decreased by a factor of $(1+A\beta)$, R_0 is increased by a factor of $(1+A\beta)$

20. Ans: (a)

Sol: Here the base emitter voltage is greater than 0.7 V and the base collector voltage is less than 0.7 V.

Hence base emitter junction is in forward bias and collector-base junction is in reverse bias.

\therefore Transistor is in forward active region

21. Ans: (d)

Sol: Here I_{CBO} doubles for every 10^0 raise in temperature V_{BE} decreases at the rate of $2.5 \text{ mV}^{\circ}\text{C}$

22. Ans: (d)

Sol: P \rightarrow RC coupled amplifier \rightarrow Audio
Q \rightarrow Differential amplifier \rightarrow DC and audio
R \rightarrow Cascode amplifier \rightarrow Video
S \rightarrow Tuned amplifier \rightarrow Narrow band

23. Ans: (d)

Sol: The oscillation frequency in crystal oscillator is determined by the crystal dimensions. This means that crystal oscillator frequency depends on all of the above parameters i.e. thickness of crystal, angle of cut and physical size of crystal

24. Ans: (a)

Sol: The transistor with comparatively small β is used in power amplifier because to handle large currents base of the transistor is made thicker. Hence β should be small



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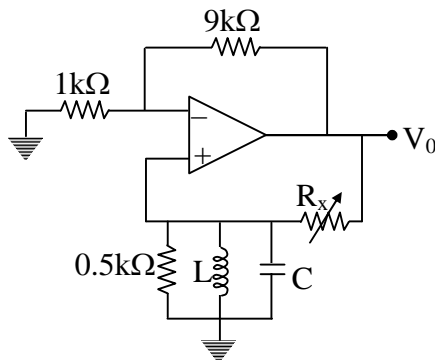
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25. Ans: (d)

Sol:



At sustained oscillations loop gain $|\beta A| = 1$
At sustained oscillations (at resonance L-C circuit acts as open circuit).

$$\beta = \frac{V_f}{V_o} = \frac{0.5k}{R_x + 0.5k} \quad \& \quad A = \left[1 + \frac{9k}{1k} \right]$$

$$\text{As } |\beta A| = 1 \Rightarrow R_x = 4.5k\Omega$$

26. Ans: (c)

Sol: The upper cross-over voltage is

$$V_{TH} = +V_{sat} \left(\frac{R_1}{R_1 + R_2} \right) = +10 \left[\frac{10k\Omega}{10k\Omega + 90k\Omega} \right] = +1 \text{ V}$$

The lower cross-over voltage is

$$V_{TH} = -V_{sat} \left(\frac{R_1}{R_1 + R_2} \right) = -10 \left[\frac{10k\Omega}{10k\Omega + 90k\Omega} \right] = -1 \text{ V}$$

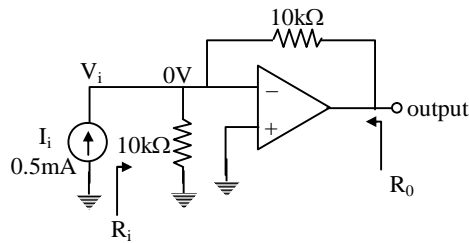
The hysteresis width is therefore

$$(V_{TH} - V_{TL}) = 1 - (-1) = 2 \text{ V}$$



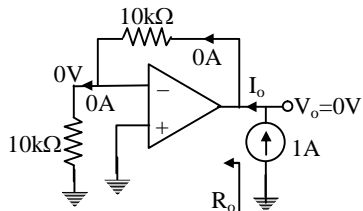
27. Ans: (b)

Sol:



$$\text{Input resistance } (R_i) = \frac{V_i}{I_i} = \frac{0}{0.5\text{m}} = 0\Omega$$

For output resistance, input current 0.5mA is open circuited & connected 1A current source at output as show in below figure.



$$\Rightarrow \text{Output resistance } (R_o) = \frac{V_o}{I_o} = \frac{0}{1} = 0\Omega$$

28. Ans (c)

Sol: The Common Emitter current gain – bandwidth product of a transistor (f_T) is defined as the frequency at which Beta of the transistor falls to unity

$$\text{Unity gain frequency } (f_T) = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

29. Ans: (a)

Sol: The bias stability of an Emitter-Bias Amplifier circuit improves by decreasing the value of R_B and increasing the value of R_E .

30. Ans: (d)

Sol: $A_V = -g_m r_{o1}$

$$= \frac{-I_{EE}/2}{V_t} \left[\frac{V_A}{I_{EE}/2} \right]$$

$$= \frac{-V_A}{V_t} = \frac{-5}{0.026} = -192.31$$

31. Ans: (d)

Sol: In current series feedback output current is proportional to input voltage. Hence it is Transconductance amplifier.

32. Ans: (a)

33. Ans: (b)

34. Ans: (a)

Sol: In PLA \Rightarrow both “AND” and “OR” programmable

(iii) represents Fan out

(iv) The basic circuit a TTL represents is a NAND gate.

35. Ans: (b)

Sol: $2^N \geq (\text{no of digits in sequence}) + 1$

N: number of flip-flops

$$2^N \geq 5 + 1$$

$$N = 3$$

So number of flip-flops = 3

36. Ans: (d)

Sol: All three are major applications

37. Ans: (a)

Sol: Using SOP form

$$\begin{aligned} Y &= \bar{A} \bar{B} (1) + \bar{A} B (1) + A \bar{B} + AB(B) \\ &= \bar{A} \bar{B} + \bar{A} B + A \bar{B} + AB \\ &= 1 \end{aligned}$$

Using POS form

$$\begin{aligned} Y &= (A + B + 1)(A + \bar{B} + 1)(\bar{A} + B + A)(\bar{A} + \bar{B} + B) \\ &= (1)(1)(1)(1) \\ &= 1 \end{aligned}$$



38. Ans: (b)

Sol:
$$x \oplus y = \overline{x \odot y}$$

$$= \overline{xy + \overline{x} \overline{y}}$$

$$= \overline{0 + \overline{x} \overline{y}}$$

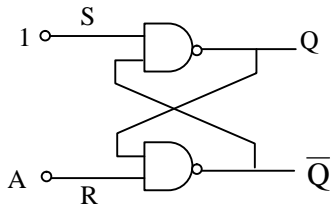
$$= \overline{\overline{x} \overline{y}}$$

$$= x + y$$

OR gate

39. Ans: (d)

Sol: Though oscillations are there when switch is closed, we need to get constant waveform without oscillations (bounce)



Fix 'S' at logic '1', connect A to 'R' input of S-R NAND latch

When $A = 0 \Rightarrow R = 0 \Rightarrow \overline{Q} = 1 \Rightarrow Q = 0$

Now, even if $A = 1$ (due to bounce) i.e $R = 1$

$\Rightarrow Q$ remains in previous state i.e., ($Q = 0$)

40. Ans: (a)

Sol:

| D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | X | Y | Z |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$Z = D_1 + D_3 + D_5 + D_7$$

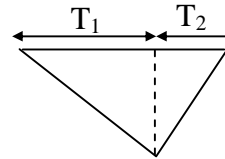
41. Ans: (c)

Sol: $(V_{in}) \cdot T_1 = (V_{ref}) \cdot T_2$

$(1) (10 \times 20 \text{msec}) = (2) T_2$

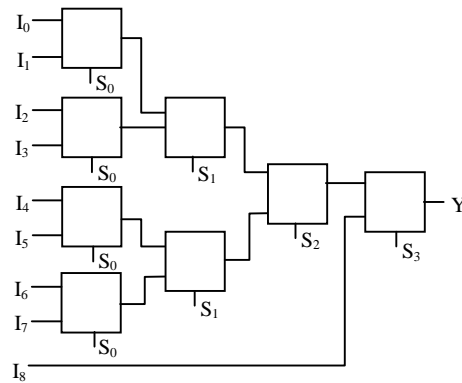
$T_2 = 100 \text{msec}$

Total time = $T_1 + T_2 = 0.3 \text{sec}$



42. Ans: (c)

Sol: Implementation is as shown



43. Ans: (d)

Sol:
$$X = (P + Q + R)(\overline{P} + \overline{Q} + \overline{R})$$

$$= PQ + P\overline{R} + \overline{P}Q + Q + Q\overline{R} + \overline{P}R + QR$$

$$= Q(1 + P + \overline{P} + \overline{R} + R) + \overline{P}R + \overline{P}R$$

$$= (P \oplus R) + Q$$

44. Ans: (d)

45. Ans: (b)

Sol:
$$\sqrt{3r^2 + r + 1} = r + 4$$

$$3r^2 + r + 1 = r^2 + 8r + 16$$

$$2r^2 - 7r - 15 = 0$$

$$2r^2 - 10r + 3r - 15 = 0$$

$$2r(r - 5) + 3(r - 5) = 0$$

$$(r - 5)(2r + 3) = 0$$

$$r = 5 \quad \text{or} \quad -1.5 \text{ (invalid)}$$

46. Ans: (b)

Sol: XOR operation gives output HIGH, when odd no. of input variables are HIGH. So, by



looking at the truth table. Option 1 and 3 are correct.

| | | | | | |
|----|----|----|----|----|----|
| | CD | 00 | 01 | 11 | 10 |
| AB | | | | | |
| | 00 | | 1 | | 1 |
| | 01 | 1 | | 1 | |
| | 11 | | 1 | | 1 |
| | 10 | 1 | | 1 | |

47. Ans: (a)

Sol: Cache memory is a very high speed memory that is placed between the CPU and main memory. The cache stores the copies of the data from frequently used main memory locations

Memory Interleaving: main memory is divided into two or more sections. The CPU can access alternate sections immediately without waiting for memory to catch up (through wait states)

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- ⊗ Detailed solutions are available.
- ⊗ **All India rank** will be given for each test.
- ⊗ Comparison with all India toppers of **ACE** students.

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48. Ans: (c)

49. Ans: (c)

Sol: CMOS inverter is formed by the series connection of one n-channel and one p-channel MOS transistor

Whereas transmission gate is formed by the parallel connection of one p-channel and one n-channel MOS transistors

50. Ans: (b)

51. Ans: (a)

52. Ans: (b)

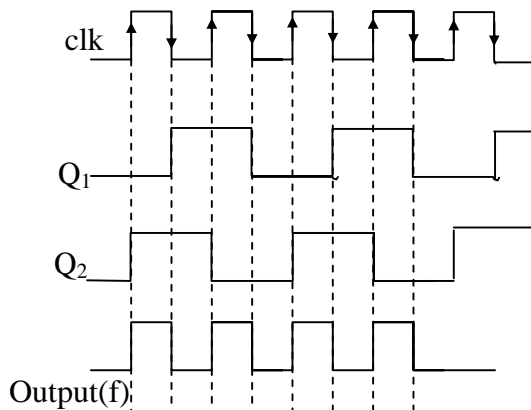
Sol:

| Clkpulse | Input | Q ₃ | Q ₂ | Q ₁ |
|----------|-------|----------------|----------------|----------------|
| 0 | | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 2 | 1 | 1 | 1 | 0 |
| 3 | 1 | 1 | 1 | 1 |
| 4 | 0 | 0 | 1 | 1 |
| 5 | 0 | 0 | 0 | 1 |
| 6 | 0 | 0 | 0 | 0 |

$\overline{Q_1}$ is fed as input in Johnson counter

53. Ans: (a)

Sol:



Output is same as clk

∴ The frequency of output is 50MHz

54. Ans: (a)

$$\text{Sol: } f_{\max} = 10\text{MHz} = \frac{1}{n \cdot t_{\text{pdf}}}$$

$$10\text{MHz} = \frac{1}{n(12.5)}$$

$$n = \frac{1}{10\text{MHz} \times 12.5\text{ns}}$$

$$n = 8$$

$$\text{Modulus} = 2^8 = 256$$

55. Ans: (c)

Sol: The time taken for SIPO is $T_1 = NT$

The time taken for SISO is

$$T_2 = (2N-1) T$$

$$T_2 - T_1 = (N-1) T$$

56. Ans: (c)

Sol: (a) & (b) are operations performed when RESET IN is made low

(c) is performed when RESET out is made high

(d) is performed during DMA data transfer

57. Ans: (b)

58. Ans: (a)

Sol: A 01

A 00, (Cy = 0, AC = 0)

Loop: A FF (bit carry flag is not affected)

JC loop is failed

Hence HLT is executed

59. Ans: (b)

Sol: ADD M ⇒ All flags affected

CMP M ⇒ All flags affected

DCR M ⇒ Except carry flag, all flags are affected

RAL ⇒ Only carry flag is affected

60. Ans: (b)



61. Ans: (d)

```
Sol: 0100 MVI A, 00H
      0102 LXI H, 0105H
      0105 OUT 00H
      0106 INR A
      0107 PCHL
      0108 HLT
```

| | | |
|-----------|-----------|-----------|
| A ← 00 | | |
| HL ← 0105 | 01 → [00] | 02 → [00] |
| A → [00] | A ← 02 | A ← 03 |
| A ← 01 | PC ← 0105 | ← 0105 |
| PC ← 0105 | | |

Infinite loop

62. Ans: (a)

Sol: Given $A + A\bar{B} + A\bar{B}C$
 $= A(1 + \bar{B} + \bar{B}C) = A$

No NAND gate is required to implement the expression

63. Ans: (c)

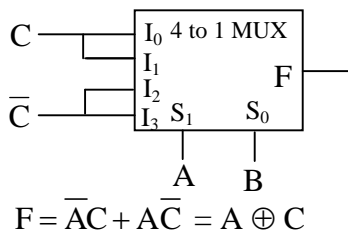
Sol: $F_1.F_2 = \Sigma m(4,6) + d(1,2,3,7)$

↓
(common minterms of F_1, F_2)

$F_1 + F_2 = \Sigma m(0,1,2,3,4,6) + d(7)$
 $(F_1.F_2) + (F_1 + F_2) = \Sigma m(0,1,2,3,4,6) + d(7)$
d.0 = 0
d.d = d
1.d = d
d+d = d
1+d = 1
0+d = d

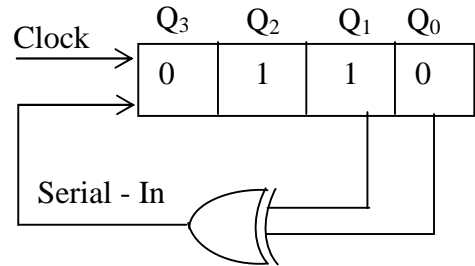
64. Ans: (d)

Sol:



65. Ans: (c)

Sol:

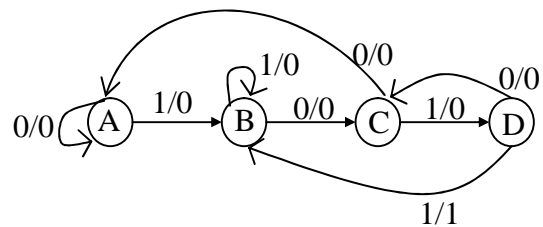


$Serial\ In = Q_1 \oplus Q_0$

| CLK | Serial In | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
|-----|-----------|----------------|----------------|----------------|----------------|
| | | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 1 | 1 | 0 | 1 | 0 |

66. Ans: (c)

Sol: The state diagram to detect the sequence 1011 is given below.



Total no. of states are = 4.
 \therefore 2 flip flops are required to detect the sequence 1011

67. Ans: (c)

Sol: Given, $N = 8E$

$V_{ref} = 10$
 $V_o = \frac{V_{ref}}{2^N} \sum_{j=0}^{N-1} 2^j b_j$

Digital input = 10100001

$\therefore V_o = \frac{10}{2^8} [1 + 2^5 + 2^7]$

$V_o = 6.289\ V$



68. Ans: (c)

Sol: TRAP has both edge & level sensitive.

69. Ans: (d)

Sol: The given memory chip size = 8K
 $= 8 \times 1024 = 2^3 \times 2^{10} = 2^{13}$
13 address lines.

70. Ans: (c)

Sol: Vector Address for RST 4.5 = 4.5×8
 $= 36$
 $= 0024 \text{ H}$

71. Ans: (b)

Sol: The gain of the CE amplifier at low frequencies depend on the coupling, bypass and blocking capacitors and independent of interelectrode capacitances. (C_{π}, C_{μ})

72. Ans: (a)

73. Ans: (b)

Sol: Both A & R are individually true, but R is not the correct explanation

74. Ans: (a)

75. Ans: (d)

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| 1 EC PRAMOD | 1 ME SUDHEER | 1 ME HASAN ASIF | 1 EE SHYAM SINGH | 1 CE NARAJA KARESH | 1 CS DEVAL N PATEL | 1 IN NAVEEN | 2 EC SREE KALYANI |
| 2 CE PUNEET KHARNA | 2 IN RAHUL MAHATO | 2 IN SHUBHAM BANSAI | 2 PI GAURAV BHADURJAL | 3 EC KARUN | 3 EE RAVI TEJA | 3 ME PRADIP DOBADI | 3 CS RAVI SHANKAR |
| 3 CE ANILKUR TRIPATHI | 4 EC SONU SHARMA | 4 EE SARFRAJ NAWAZ | 4 CE CHIRAG MITTAL | 4 ME GAUSH ALAM | 4 IN MONTI | 4 PI SanghaviPr Adhikari | 5 IN VRAJESH SHAH |
| 5 PI ANKIT TIWARI | 6 EC LROSTA SAI LIPPU | 6 CS MEGHASHAYAM | 6 EE RAJAKESHAR REDDY | 6 IN RAMESH KAVULLA | 6 PI PINAL KUMAR RANA | 7 IN PARRAJ AISHRA | 8 ME DIVYANSHU JHA |
| 8 PI Mona Bhargava | 9 EC Anand Upadhi | 9 CS Nihar Ranjan Mishra | 9 ME DHEEPA KUMAR JHA | 10 EC AMIT KAWAT | 10 ME ANAND SETHI | 10 EE SURAJ DASH | 10 IN KIRAN SURESHKAR |

ESE TOPPERS

ESE 2017

| CE | | E&T | | EE | | ME | |
|---|-----------------------------|--|------------------------------------|--|---------------------------|---|---------------------------|
| 1 CE NAMIT JAIN | 2 CE PRAVIND SINGH | 2 E&T DIVYANSHU CHAUDHARY | 3 E&T SRIHARSHI MENYANAGULLU | 2 EE PREETI KUMARI | 3 EE KARAGODDARI | 3 ME SAURABH | 4 ME AMIT KUMAR RAN |
| 3 CE ANKIT | 6 CE BHASKAR BANERJEE | 5 E&T ANANT GAUTAM | 6 E&T SUBHANGINI MISHRA | 4 EE HARSHIT KUMAR SINGH | 5 EE NIGEL KUMAR | 6 ME ANJAN GUPTA | 7 ME DHRUV JHA |
| 8 CE ADITYA SINGH | 9 CE HIMANSHU GAUTAM | 7 E&T DEVANURAGH DRAWN KUMAR | 8 E&T DEEPAJ GOYAL | 6 EE DUSHYANT SINGH | 8 EE ARPOORVA GUPTA | 9 ME ACHARAJ GUPTA | |
| 10 CE AYUSH DUBEY | 7 IN TOP 10 RANKS | 9 E&T ABHIRAM PRADYPSINGH | 10 E&T UMESH | 9 EE KIRAN BABU KONERU | | | 5 IN TOP 10 RANKS |
|  7 All India 1 st Rank in ESE. | | 8 IN TOP 10 RANKS and many more... | | 7 IN TOP 10 RANKS | |  27 Ranks in Top 10 in ESE-2017 | |



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