



# ACE

## Engineering Academy



Hyderabad | Delhi | Bhopal | Pune | Bhubaneswar | Bengaluru | Lucknow | Patna | Chennai | Vijayawada | Visakhapatnam | Tirupati | Kukatpally | Kolkata

H.O: 204, II Floor, Rahman Plaza, Opp. Methodist School, Abids, Hyderabad-500001,

Ph: 040-23234418, 040-23234419, 040-23234420, 040 - 24750437

### ESE- 2018 (Prelims) - Offline Test Series-Test-1

### ELECTRICAL ENGINEERING

## SUBJECT: ANALOG AND DIGITAL ELECTRONICS + BASIC ELECTRONICS

### ENGINEERING – SOLUTIONS

**01. Ans: (c)**

**Sol:** The given circuit is a wein-bridge oscillator  
The condition for sustained oscillations (or) the minimum voltage gain required to maintain the oscillations in a wein-Bridge oscillator is

$$A_V = 1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} \text{ ----- (1)} \quad [\text{where } R_1 =$$

$2R, R_2 = R, C_1 = C \text{ and } C_2 = 2C \text{ in the given circuit}]$

$$\Rightarrow 1 + \frac{R_f}{R_1} = 1 + \frac{2R}{R} + \frac{2C}{C} = 5 \text{ ----- (2)}$$

$$\Rightarrow R_f/R_1 = 4 \text{ ----- (3)}$$

$$\therefore R_f = 4R_1 \text{ -----(4)}$$

**02. Ans: (c)**

**Sol: Step (1):**

$$\text{When } V_i = -2V, V_A = -12V$$

**Step (2):**

$$\therefore V_A = -12V, D \text{ is OFF} \Rightarrow V_0 = 0V$$

**03. Ans: (d)**

**Sol:** Step (1): KCL at collector node of  $Q_1$

$$I_{Ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1} + 2I_{B_2}$$

$$= I_{C_2} + \frac{2I_{C_2}}{\beta}$$

$$= I_{C_2} \left[ 1 + \frac{2}{\beta} \right]$$

$$\therefore \frac{I_{Ref}}{I_{C_2}} = \frac{I_{Ref}}{I_0} = 1 + \frac{2}{50} = 1.04$$

**04. Ans: (b)**

**Sol:** Step (1):

$$f_{L_f} = \frac{f_L}{1 + A\beta} = \frac{2\text{kHz}}{1 + 1000 \times 0.01} = 181.818\text{Hz}$$



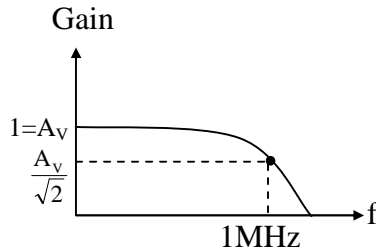
Step (2):

$$f_{H_f} = f_H (1 + A\beta)$$

$$= 20\text{kHz} \times (1 + 1000 \times 0.01) = 220\text{kHz}$$

05. Ans: (b)

Sol:



$$\text{Bandwidth} = f_H = 1\text{MHz}$$

$$\text{At } f_H, \text{ Gain of the amplifier, } A_v = \frac{1}{\sqrt{2}}$$

$$\Rightarrow A_v = \frac{V_0}{V_i} = \frac{1}{\sqrt{2}} V$$

$$V_0 = \frac{V_i}{\sqrt{2}} = \frac{2}{\sqrt{2}} = \sqrt{2} V$$

06. Ans: (a)

07. Ans: (b)

08. Ans: (b)

Sol: In negative feedback amplifiers

Voltage gain ↓

Bandwidth ↑

Noise ↓

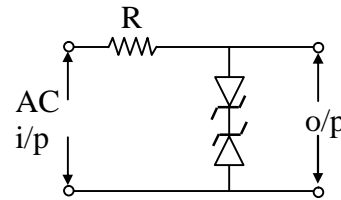
Distortion ↓

Amplitude fluctuations ↓

09. Ans: (a)

10. Ans: (d)

Sol:



11. Ans: (a)

$$\text{Sol: } V_H = 2V_{\text{sat}} \left( \frac{R_2}{R_1 + R_2} \right)$$

$$= 2 \times 10 \left( \frac{1}{1+9} \right) = 2V$$

12. Ans: (c)

Sol:  $V_0 = \text{gain} \times \text{input voltage}$

$$= A \times V_m \sin \omega t \quad (\text{i.e., } A \times V_m = V_x)$$

$$\frac{dV_0}{dt} = V_x \cos \omega t \times \omega$$

$$SR = \left. \frac{dV_0}{dt} \right|_{\text{max}} = V_x 2\pi f$$

$$\Rightarrow 100 \times 10^6 = V_x \times 2\pi \times 20 \times 10^6$$

$$V_x = \frac{100}{40\pi} = \frac{5}{2\pi} V$$

13. Ans: (c)

Sol:  $V_0 = -2(2) = -4V$

$$I_0 = -\frac{V_0}{2k} + \left( \frac{-V_0}{1k} \right)$$

$$= 2 \times 10^{-3} + 4 \times 10^{-3}$$

$$= 6 \text{ mA}$$

# Pre GATE-2018

COMPUTER BASED TEST

Date of Exam : 20<sup>th</sup> Jan 2018

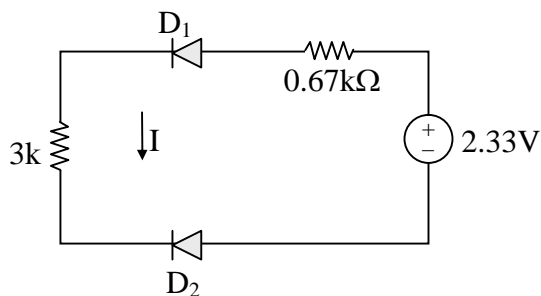
Last Date To Apply : 05<sup>th</sup> Jan 2018

www.aceenggacademy.com

14. Ans: (a)

Sol: both the diodes are OFF

$$I = 0$$

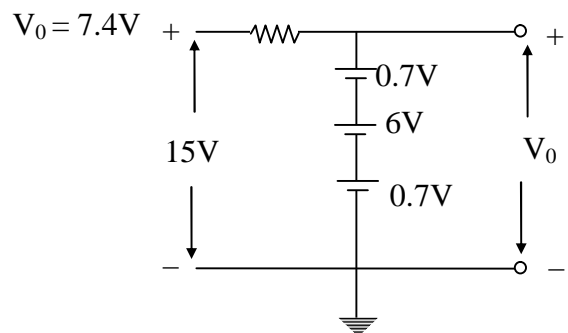


15. Ans: (c)

Sol: D → F B

Z<sub>1</sub> → operated in break down region

Z<sub>2</sub> → F B then



16. Ans: (b)

17. Ans: (d)

$$\text{Sol: } V_0 = \frac{R_2}{R_1} \times (V_1 - V_2)$$

$$V_1 - V_2 = -2V$$

$$V_0 = 5(-2) \\ = -10V$$



**18. Ans: (a)**

**Sol:** For negative feedback, gain factor is reduced by  $(1 + A\beta)$  for shunt-series,  $R_{in}$  is decreased by a factor of  $(1+A\beta)$ ,  $R_o$  is increased by a factor of  $(1 + A\beta)$

**19. Ans: (a)**

**Sol:** Here the base emitter voltage is greater than 0.7 V and the base collector voltage is less than 0.7 V.

Hence base emitter junction is in forward bias and collector-base junction is in reverse bias.

$\therefore$  Transistor is in forward active region

**20. Ans: (d)**

**Sol:** Here  $I_{CBO}$  doubles for every  $10^0$  raise in temperature  $V_{BE}$  decreases at the rate of  $2.5 \text{ mV}/^\circ\text{C}$

**21. Ans: (d)**

**Sol:** P  $\rightarrow$  RC coupled amplifier  $\rightarrow$  Audio

Q  $\rightarrow$  Differential amplifier  $\rightarrow$  DC and audio

R  $\rightarrow$  Cascode amplifier  $\rightarrow$  Video

S  $\rightarrow$  Tuned amplifier  $\rightarrow$  Narrow band

**22. Ans: (d)**

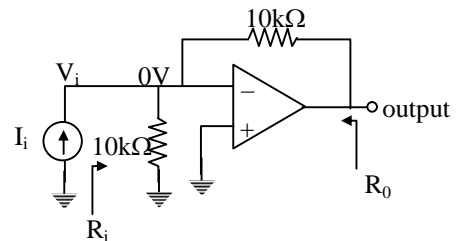
**Sol:** The oscillation frequency in crystal oscillator is determined by the crystal dimensions. This means that crystal oscillator frequency depends on all of the above parameters i.e. thickness of crystal, angle of cut and physical size of crystal

**23. Ans: (a)**

**Sol:** The transistor with comparatively small  $\beta$  is used in power amplifier because to handle large currents base of the transistor is made thicker. Hence  $\beta$  should be small

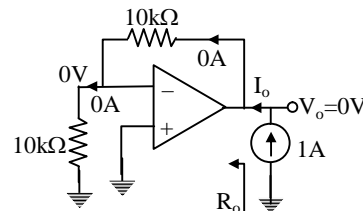
**24. Ans: (b)**

**Sol:**



$$\text{Input resistance } (R_i) = \frac{V_i}{I_i} = \frac{0}{0.5\text{m}} = 0\Omega$$

For output resistance, input current 0.5mA is open circuited & connected 1A current source at output as show in below figure.



$$\Rightarrow \text{Output resistance } (R_o) = \frac{V_o}{I_o} = \frac{0}{1} = 0\Omega$$

**25. Ans (c)**

**Sol:** The Common Emitter current gain – bandwidth product of a transistor ( $f_T$ ) is defined as the frequency at which Beta of the transistor falls to unity



$$\text{Unity gain frequency } (f_T) = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

**26. Ans: (a)**

**Sol:** The bias stability of an Emitter-Bias Amplifier circuit improves by decreasing the value of  $R_B$  and increasing the value of  $R_E$ .

**27. Ans: (d)**

**Sol:**  $A_V = -g_m r_{o1}$

$$= \frac{-I_{EE}/2}{V_t} \left[ \frac{V_A}{I_{EE}/2} \right]$$

$$= \frac{-V_A}{V_t} = \frac{-5}{0.026} = -192.31$$

**28. Ans: (d)**

**Sol:** In current series feedback output current is proportional to input voltage. Hence it is Transconductance amplifier.

**29. Ans: (a)**

**Sol:** When two pure conductors are added then resistivity increases at all time

**30. Ans: (c)**

**Sol:**  $\lambda_{\max} = \frac{1.24}{E_G \text{ (eV)}} \mu\text{m}$

$$= \frac{1.24}{2.5} \mu\text{m} = 0.496 \mu\text{m} = 4960 \text{ \AA}$$

**31. Ans: (a)**

**Sol:** Junction capacitance  $\propto \frac{1}{\text{Junction Voltage}}$

Step:  $C_j \propto \frac{1}{\sqrt{V_s}} \rightarrow \frac{1}{2}$

Linear:  $C_j \propto \frac{1}{\sqrt[3]{V_s}} \rightarrow \frac{1}{3}$

Diffused =  $C_j \propto \frac{1}{\sqrt[2.5]{V_s}} \rightarrow \frac{1}{2.5}$

**32. Ans: (b)**

**Sol:** Voltage shunt feed back

**33. Ans: (b)**

**Sol:**  $I_D = I_{DSS} \left( 1 - \frac{V_{gs}}{V_p} \right)^2$

Transconductance of ( $g_m$ ) FET is

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{2I_{DSS}}{-V_p} \left( 1 - \frac{V_{gs}}{V_p} \right)$$

$$\left[ \because \left( 1 - \frac{V_{gs}}{V_p} \right)^2 = \frac{I_D}{I_{DSS}} \right]$$

$$g_m = \frac{2}{|V_p|} \sqrt{I_D \cdot I_{DSS}}$$



# ESE | GATE - 2019

## LONG TERM BATCHES

EC | EE | ME | CE | CS | IN | PI

*Start Early, Gain Surely*



Pioneer to  
Leader



Dedicated  
Service



Experienced Faculty  
from Central Pool

Admissions are open at all our centers

H. O. : Hyderabad : Ph : 040-23234418,19,20

Bangalore  
9341299966

Kukatpally  
040-6597 4465

Delhi  
9205282121

Bhopal  
0755-2554512

Pune  
020-25535950

Bhubaneswar  
0674-2540340

Lucknow  
808199966

Patna  
9308699966

Chennai  
044-42123289

Vijayawada  
0866-2490001

Vishakapatnam  
0891-6616001

Tirupathi  
0877-2244388

Kolkata  
8297899966

**34. Ans: (d)**

**Sol:** Once an SCR is turned on, it will remain so until the anode current goes below to holding current value.

**35. Ans: (d)**

**Sol:** LED is made by a direct band gap material.

$$E_g = \frac{hc}{\lambda}$$

The colour of the light has a particular wavelength  $\lambda$  according to the band gap energy of semiconductor material

**36. Ans: (a)**

**Sol:** The auto correlation function of White Noise is a delta function.

$$\delta(t) \left\langle \frac{FT}{Pair} \right\rangle 1$$

$$\text{So } \frac{N_0}{2} \delta(t) \left\langle \frac{FT}{Pair} \right\rangle \frac{N_0}{2}$$

**37. Ans: (c)**

**Sol:**  $P_c = 1.8 \text{ KW}$

$$P_{SB} = \frac{P_c \mu^2}{4} = 200 \text{ W}$$

$$\frac{1.8 \times 10^3 \times \mu^2}{4} = 200 \text{ W}$$

$$\mu^2 = 4/9$$



$$\mu = \sqrt{\frac{4}{9}} = \frac{2}{3} = 0.666$$

$$\% \mu = 66.66\%$$

**38. Ans: (c)**

**Sol:** modulation index of AM

$\mu = k_a A_m$  which is independent of frequency

$$\text{FM } \beta_f = \frac{k_f A_m}{f_m}$$

$f_m$  doubled,  $\beta_f$  is half

PM  $\beta_p = k_p A_m$ , independent of frequency

**39. Ans: (b)**

**Sol:** For entropy of source

$$S_1 = \log_2 4 = 2 \log_2 2$$

$$= 2 \text{ bits/symbol}$$

For entropy or source

$$S_2 = \log_2 16 = 4 \log_2 2$$

$$= 4 \text{ bits/symbol}$$

**40. Ans: (b)**

**Sol:** If  $L = 2 \rightarrow$  Data word length  $n = 1$  bit.

$$\text{Data rate} = n f_s \text{ b/sec}$$

$$= f_s \text{ bits/sec,}$$

Where  $f_s$  is the sampling rate.

If  $L = 8 \rightarrow n = 3$  bits.

$$\text{Data rate} = 3f_s \text{ bps.}$$

Since (B.W)  $\propto$  data rate, B.W requirement gets tripled.

**41. Ans: (b)**

**Sol:** The signal is received using the pre-selection stage, i.e. an RF amplifier. It is mixed with local oscillator and IF is generated. It is amplified by the IF amplifier and the amplitude variations are removed by amplitude limiter. Then, it is applied to the FM demodulator. The demodulated signal is amplified by an audio amplifier.

**42. Ans: (c)**

**Sol:** Typical Uplink & Downlink frequencies used in satellite communication are

Uplink	Downlink
6 GHz	4 GHz
14 GHz	12 GHz
30 GHz	24 GHz

**43. Ans: (d)**

**Sol:** Flash memory takes more number of Read/Write cycles

**44. Ans: (a)**

**Sol:** In PLA  $\Rightarrow$  both "AND" and "OR" programmable  
(iii) Represents Fan out

**45. Ans: (b)**

**Sol:**  $2^N \geq$  (no of digits in sequence) + 1

N: number of flip-flops



$$2^N \geq 5 + 1$$

$$N = 3$$

So number of flip-flops = 3

**46. Ans: (a)**

**Sol:** Using SOP form

$$\begin{aligned} Y &= \bar{A} \bar{B} (1) + \bar{A} B (1) + A \bar{B} + AB(B) \\ &= \bar{A} \bar{B} + \bar{A} B + A \bar{B} + AB \\ &= 1 \end{aligned}$$

Using POS form

$$\begin{aligned} Y &= (A + B + 1)(A + \bar{B} + 1)(\bar{A} + B + A)(\bar{A} + \bar{B} + B) \\ &= (1)(1)(1)(1) \\ &= 1 \end{aligned}$$

**47. Ans: (b)**

**Sol:**  $x \oplus y = \overline{x \odot y}$

$$\begin{aligned} &= \overline{xy + \bar{x}\bar{y}} \\ &= \overline{0 + \bar{x}\bar{y}} = \overline{\bar{x}\bar{y}} = x + y \end{aligned}$$

OR gate

**48. Ans: (a)**

**Sol:**

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

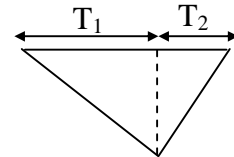
$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$Z = D_1 + D_3 + D_5 + D_7$$

**49. Ans: (c)**

**Sol:**



$$(V_{in}) \cdot T_1 = (V_{ref}) \cdot T_2$$

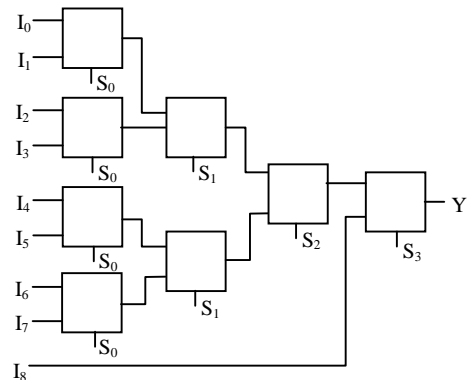
$$(1) (10 \times 20 \text{msec}) = (2) T_2$$

$$T_2 = 100 \text{msec}$$

$$\text{Total time} = T_1 + T_2 = 0.3 \text{sec}$$

**50. Ans: (c)**

**Sol:** Implementation is as shown





**GATE - 2018**

**ONLINE TEST SERIES**

**No. of Tests : 62**

All tests will be available till  
12<sup>th</sup> February 2018

**ESE - 2018 PRELIMS**

**ONLINE TEST SERIES**

**No. of Tests : 44**

All tests will be available till  
07<sup>th</sup> January 2018

**ISRO - 2017**

**ONLINE TEST SERIES**

**No. of Tests : 15**

All tests will be available till  
25<sup>th</sup> December 2017

★ HIGHLIGHTS ★

- Detailed solutions are available.
- **All India rank** will be given for each test.
- Comparison with all India toppers of **ACE** students.

 [www.aceenggacademy.com](http://www.aceenggacademy.com)

 [testseries@aceenggacademy.com](mailto:testseries@aceenggacademy.com)

**51. Ans: (d)**

$$\begin{aligned}\text{Sol: } X &= (P + Q + R)(\bar{P} + Q + \bar{R}) \\ &= PQ + P\bar{R} + \bar{P}Q + Q + Q\bar{R} + \bar{P}R + QR \\ &= Q(1 + P + \bar{P} + \bar{R} + R) + \bar{P}R + \bar{P}R \\ &= (P \oplus R) + Q\end{aligned}$$

**52. Ans: (b)**

$$\begin{aligned}\text{Sol: } \sqrt{3r^2 + r + 1} &= r + 4 \\ 3r^2 + r + 1 &= r^2 + 8r + 16 \\ 2r^2 - 7r - 15 &= 0 \\ 2r^2 - 10r + 3r - 15 &= 0 \\ 2r(r - 5) + 3(r - 5) &= 0 \\ (r - 5)(2r + 3) &= 0\end{aligned}$$

$$r = 5 \quad \text{or} \quad -1.5 \text{ (invalid)}$$

**53. Ans: (b)**

**Sol:** XOR operation gives output HIGH, when odd no. of input variables are HIGH. So, by looking at the truth table. Option 1 and 3 are correct.

CD	00	01	11	10
AB				
00		1		1
01	1		1	
11		1		1
10	1		1	



54. Ans: (a)

**Sol:** Cache memory is a very high speed memory that is placed between the CPU and main memory. The cache stocks the copies of the data from frequently used main memory locations

**Inter leaving:** main memory is divided into two or more sections. The CPU can access alternate sections immediately without waiting for memory to catch up (through wait states)

55. Ans: (c)

**Sol:** CMOS inverter is formed by the series connection of one n-channel and one p-channel MOS transistor

Whereas transmission gate is formed by the parallel connection of one p-channel and one n-channel MOS transistors

56. Ans: (a)

57. Ans: (b)

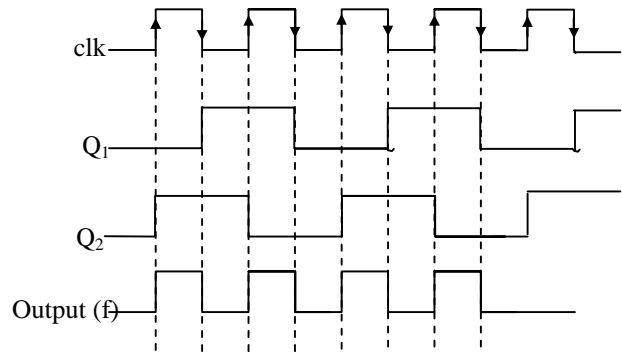
**Sol:**

Clk pulse	Input	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>
0		0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	0	1	1
5	0	0	0	1
6	0	0	0	0

$\overline{Q_1}$  is fed as input in Johnson counter

58. Ans: (a)

**Sol:**



Output is same as clk

∴ The frequency of output is 50MHz

59. Ans: (c)

**Sol:**  $F_1.F_2 = \Sigma m(4,6) + d(1, 2, 3, 7)$

↓  
(common minterms of  $F_1, F_2$ )

$$F_1 + F_2 = \Sigma m(0, 1, 2, 3, 4, 6) + d(7)$$

$$(F_1.F_2) + (F_1 + F_2) = \Sigma m(0,1,2,3,4,6) + d(7)$$

$$d.0 = 0$$

$$d.d = d$$

$$1.d = d$$

$$d + d = d$$

$$1 + d = 1$$

$$0 + d = d$$



**60. Ans: (c)**

**Sol:** the time taken for SIPO is

$$T_1 = NT$$

The time taken for SISO is

$$T_2 = (2N-1) T$$

$$T_2 - T_1 = (N-1) T$$

**61. Ans: (c)**

**Sol:** (a),(b) are operations Performed when RESETIN is made low

(c) is performed when RESET out is made high

(d) is performed during DMA data transfer

**62. Ans: (d)**

**Sol:** 0100 MVI A, 00H

0102 LXI H, 0105H

0105 OUT 00H

0106 INR A

0107 PCHL

0108 HLT

A ← 00		
HL ← 0105	01 → [00]	02 → [00]
A → [00]	A ← 02	A ← 03
A → 01	PC ← 0105	PC ← 0105
PC ← 0105		

Infinite Loop

**63. Ans: (a)**

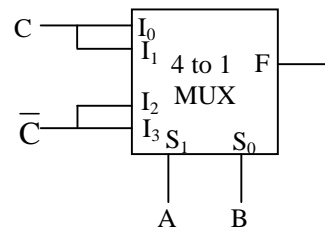
**Sol:** Given  $A + A\bar{B} + A\bar{B}C$

$$= A(1 + \bar{B} + \bar{B}C) = A$$

No NAND gate is required to implement the expression

**64. Ans: (d)**

**Sol:**



$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC$$

$$F = \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$$

$$F = \bar{A}C + A\bar{C} = A \oplus C$$

# GATE TOPPERS

GATE  
2017

1 EC PRAMOD	1 ME SUDHEER	1 ME HASAN ASIF	1 EE SHYAM SINGH	1 CE WIKAL PARESH	1 CS DEVAL N PATEL	1 IN NAVEEN	2 EC SREE KALYANI
2 CE PUNEET KHANNA	2 IN RAHUL MAHATO	2 IN SHUBHAM BANSAL	2 PI GAURAV DHARDOJAL	3 EC KARUN	3 EE RAVI TEJA	3 ME PRADEP BOBAGE	3 CS RAVI SHANKAR
3 CE ANKUR TRIPATHI	4 EC SONU SHARMA	4 EE SARFRAJ NAWAZ	4 CE CHIRAG MITTAL	4 ME GAUSH ALAM	4 IN MONTI	4 PI Sangeetha Adhikari	5 IN VRAJESH SHAH
5 PI ANKIT TIWARI	6 EC LISHA SAI LIPPU	6 CS MEGHASHPATAM	6 EE RAJASEKHAR REDDY	6 IN RAVESH KAMALLA	6 PI PINAL KUMAR RANA	7 IN RANRAJ WISHRA	8 ME DIYANSHU JHA
8 PI Noma Banerjee	9 EC Anand Upadhye	9 CS Nikhil Anand Singh	9 ME SHRUTI KUMAR JHA	10 EC AMIT BAWAR	10 ME SIDDHANT GUPTA	10 EE SURAJ DASH	10 IN PANKAJ MISHRA

# ESE TOPPERS

ESE  
2017

CE		E&T		EE		ME	
1 CE NAMIT JAIN	2 CE PRAVIND SINGH	2 EST SUDHANSHU CHAUDHARY	3 EST KJULLAR NIRMALKUMAR	2 EE PREETI KUMARI	3 EE HARSH SINGH	3 ME SAURABH	4 ME AMIT KUMAR PAN
3 CE ANKIT	6 CE BISHAY DAVARWACH	5 EST AMIT GAUTAM	6 EST SUBIRANJAN MISHRA	4 EE HARSHIT KUMAR SINGH	5 EE NIGEL KUMAR	6 ME ANKAN GUPTA	7 ME DHRUV JHA
8 CE ADITYA SINGH	9 CE HIMANSHU GAUTAM	7 EST DEVIKURUM RAVAN KUMAR	8 EST DEEPA GUPTA	6 EE DUSHYANT SINGH	8 EE APOORVA GUPTA	9 ME ACHARAJ GUPTA	
10 CE AYUSH DUBEY	7 IN TOP 10 RANKS	9 EST AJAY SIKH PRADIP SINGH	10 EST LIMESH	9 EE NIRAN DASU KONEKU			5 IN TOP 10 RANKS
 <b>7</b> All India 1 <sup>st</sup> Rank in ESE.		<b>8</b> IN TOP 10 RANKS and many more...		<b>7</b> IN TOP 10 RANKS		 <b>27</b> Ranks in Top 10 in ESE-2017	

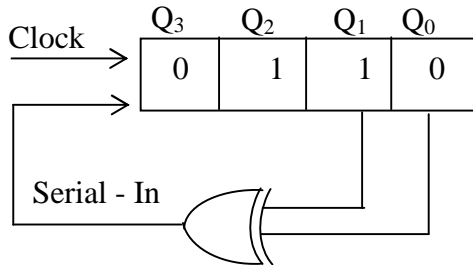


**ACE**  
Engineering Academy  
Leading Institute for ESE/GATE/PSUs



65. Ans: (c)

Sol:

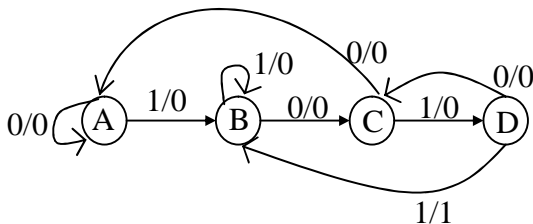


$$\text{Serial In} = Q_1 \oplus Q_0$$

CLK	Serial In	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
		0	1	1	0
1	1	1	0	1	1
2	0	0	1	0	1
3	1	1	0	1	0

66. Ans: (c)

Sol: The state diagram to detect the sequence 1011 is given below.



Total no. of states are = 4.

∴ 2 flip flops are required to detect the sequence 1011

67. Ans: (c)

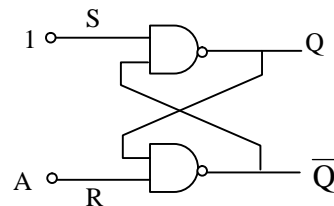
Sol: TRAP has both edge & level sensitive.

68. Ans: (c)

Sol: Vector Address for RST 4.5 =  $4.5 \times 8$   
= 36  
= 0024 H

69. Ans: (d)

Sol: though oscillations are there when switch is closed, we need to get constant waveform without oscillations (bounce)



Fix 'S' at logic '1', connect A to 'R' input of S-R NAND latch

When  $A = 0 \Rightarrow R = 0 \Rightarrow \bar{Q} = 1 \Rightarrow Q = 0$

Now, even if  $A = 1$  (due to bounce) i.e  $R = 1 \Rightarrow Q$  remains in previous state i.e., ( $Q = 0$ )



**70. Ans: (d)**

**Sol:** In BJT as temperature increasing  $I_{CO}$  increases So,  $I_c$  increases.

Where in FET, As temperature increases mobility decreases So  $I_D$  decreases and as temperature increases carrier concentration  $n_i$  increases so  $I_D$  increases.

So overall  $I_D$  will not get changed.

Thermal stability in FET is more than BJT  
Parameter variation with temperature change is less.

**71. Ans: (a)**

**Sol:** Using A S C I I, we can represent data in both numbers and characters

**72. Ans: (a)**

**73. Ans: (d)**

**74. Ans: (b)**

**Sol:** The gain of the CE amplifier at low frequencies depend on the coupling, bypass and blocking capacitors and independent of interelectrode capacitances.

**75. Ans: (a)**