



# ACE

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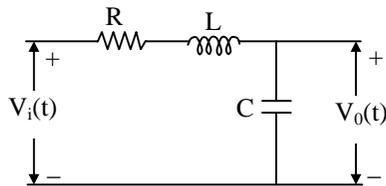
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**ESE- 2018 (Prelims) - Offline Test Series** **Test- 13**  
**ELECTRONICS & TELECOMMUNICATION ENGINEERING**

**SUBJECT: CONTROL SYSTEMS + ANALOG ELECTRONICS**  
**+ DIGITAL ELECTRONICS MICRO PROCESSOR**  
**SOLUTIONS**

**01. Ans: (d)**

**Sol:** Given circuit is shown in below figure.



$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{Cs}}{R + Ls + \frac{1}{Cs}} = \frac{1}{RCs + LCs^2 + 1}$$

CE is  $LCs^2 + RCs + 1 = 0$

$$\Rightarrow s^2 + \frac{R}{L}s + \frac{1}{LC} = 0 \dots\dots (1)$$

We know for standard second order characteristic equation

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \dots\dots (2)$$

$\zeta = 0$  for undamped system

$0 < \zeta < 1$  for under damped system

For system poles to be on real axis,  $\zeta > 1$

For system poles to be on complex plane,  $\zeta < 1$ .

Compare (1) , (2) we get

$$\omega_n = \frac{1}{\sqrt{LC}}, \zeta = \frac{R}{2} \sqrt{\frac{C}{L}}$$

For  $R = 0 \Rightarrow \zeta = 0$

For  $R = 1\Omega, L = 1H, C = 1F, \zeta = \frac{1}{2} < 1$

For  $\zeta > 1 \Rightarrow R > 2\sqrt{\frac{L}{C}}$

For  $\zeta < 1 \Rightarrow R < 2\sqrt{\frac{L}{C}}$

From all above conclusions

Statements 1, 2, 3 are correct



**02. Ans: (c)**

**Sol:** C.L.T.F. =  $\frac{s^2}{2s+1} = \frac{s^2}{1 + \frac{s^2}{2s+1}} = \frac{s^2}{s^2 + 2s + 1}$

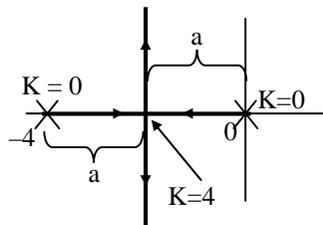
C.E is  $s^2+2s+1=0 \Rightarrow s=-1, -1 \Rightarrow$  system is critically damped.

Order of the system is two

$\therefore$  Both statements are correct.

**03. Ans: (d)**

**Sol:** Root Locus plot is as shown below



'K' at break point = (a)  $(a) = a^2$

$\Rightarrow a^2 = 4$

$\Rightarrow a = 2$

$\therefore s = -2$

System is over damped for poles on real axis i.e  $0 < k < 4$  only.

As two branches are there, so it is second order system.

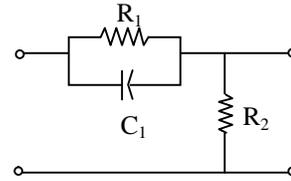
System to be under damped, poles should be on complex plane.

$\therefore 4 < k < \infty$ .

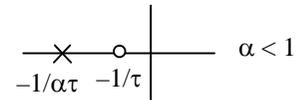
So Statements 1, 4 are true.

**04. Ans: (b)**

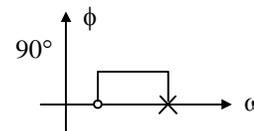
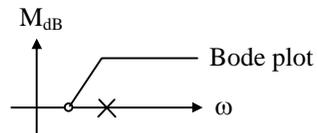
**Sol:**



TF<sub>lead</sub> =  $\frac{\tau s + 1}{\alpha \tau s + 1} \quad \alpha < 1$



It adds a dominant zero



- It adds positive phase angle
  - The system is always stable as the pole is in LHP
  - Its magnitude will vary with frequency as shown in bode plot
- $\therefore$  1, 2, 3 are correct

**05. Ans: (d)**

**Sol:** All the statements are true. Therefore correct option is (d).

**06. Ans: (a)**

**Sol:**  $k = -(s(s+4)(s^2+4s+8))$

$k = -(s^4+8s^3+24s^2+32s)$



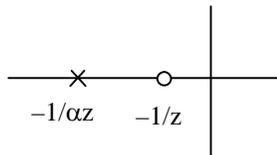
$$\frac{dk}{ds} = -(4s^3 + 24s^2 + 48s + 32) = 0$$

$$s = -2, -2, -2$$

$s = -2$  is a break point.

**07. Ans: (a)**

**Sol:** The compensator is lead



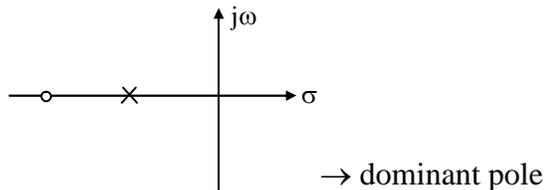
$$\omega_n = \sqrt{1 \times 10} = \sqrt{10} \text{ rad/sec}$$

The maximum phase angle is obtained at

$$\sqrt{10} \text{ rad/sec}$$

**08. Ans: (b)**

**Sol:** Lag compensator, pole-zero diagram



Lag compensator decreases  $\omega_{gc}$ , bandwidth.

**09. Ans: (c)**

$$\text{Sol: } CLTF = \frac{C(s)}{R(s)} = \frac{KG}{1 + KGH}$$

$$S_K^{CLTF} = \frac{1}{1 + KGH}$$

$$S_G^{CLTF} = \frac{1}{1 + KGH}$$

$$S_H^{CLTF} = \frac{-KGH}{1 + KGH}$$

If loop gain is high

$$KGH \rightarrow \infty$$

$$mS_K^{CLTF} = 0, S_G^{CLTF} = 0, S_H^{CLTF} = -1$$

**10. Ans: (d)**

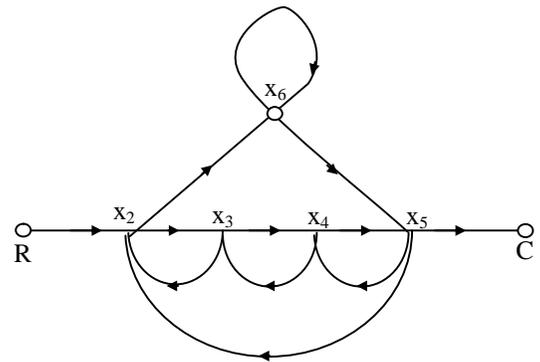
$$\text{Sol: } M_p = e^{-\pi\zeta/\sqrt{1-\zeta^2}}$$

$$\zeta = \cos\theta$$

$$= e^{-\frac{\pi \cos\theta}{\sin\theta}} = e^{-\pi \cot\theta}$$

**11. Ans: (b)**

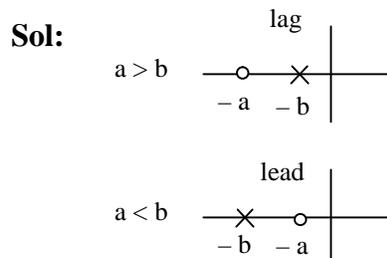
**Sol:** Given signal flow graph is as shown below



Forward paths are

$$\Rightarrow \left. \begin{aligned} &(R, x_2, x_3, x_4, x_5, C) \\ &(R, x_2, x_6, x_5, C) \end{aligned} \right\} \text{two forward paths}$$

**12. Ans: (a)**

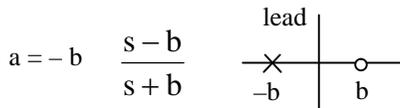




b = 0

$$G(s) = \frac{s+a}{s} = 1 + \frac{a}{s}$$

∴ PI controller



All pass system

Therefore 1,2,3,4 are correct

13. Ans: (b)

Sol: TF from root locus is  $= \frac{k}{s(s+a)(s+b)}$ ,

where a, b are +ve

- The system is 3<sup>rd</sup> order
  - It has break point between (0, -a)
  - The system will be marginally stable for some k
- There fore only 1, 2 are correct

14. Ans: (a)

Sol: Forward path going are H<sub>1</sub>G<sub>1</sub>, H<sub>2</sub>G<sub>1</sub>G<sub>2</sub>

- Loop gains are - H<sub>1</sub>G<sub>1</sub>, -H<sub>2</sub>G<sub>1</sub>G<sub>2</sub>
- Both loops are touching loops so 3 is incorrect



# Pre GATE-2018

## COMPUTER BASED TEST

Date of Exam : 20<sup>th</sup> Jan 2018

Last Date To Apply : 05<sup>th</sup> Jan 2018



**15. Ans: (b)**

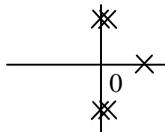
**Sol:** From RH criteria

$s^5$	1	2	1	
$s^4$	-1	-2	-1	AE <sub>1</sub>
$s^3$	(0) -4	(0) -4	0	Row of zero
$s^2$	-1	-1	0	AE <sub>2</sub>
$s^1$	(0) -2	0		Row of zero
$s^0$	-1			

No sign change below AE so all four roots of AE equation lies on  $j\omega$  axis.

$$AE = -s^4 - 2s^2 - 1 = 0$$

$$(s^2 + 1)^2 = 0$$



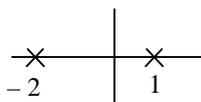
0 Poles  $\rightarrow$  LHP

4 Poles  $\rightarrow$   $j\omega$  -axis

1 Pole  $\rightarrow$  RHP (one sign change on first column)

**16. Ans: (c)**

**Sol:**  $G(s) = \frac{10}{(s-1)(s+2)}$



So,  $G(s)$  is unstable

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1+G(s)} = \frac{10}{(s-1)(s+2)+10}$$

$$= \frac{10}{s^2 - 2 + 2s - s + 10}$$

$$= \frac{10}{s^2 + s + 8}$$

$$C.E = s^2 + s + 8 = 0$$

$$s^2 \quad \left| \begin{array}{l} 1 \quad 8 \end{array} \right.$$

$$s^1 \quad \left| \begin{array}{l} 1 \quad 0 \end{array} \right.$$

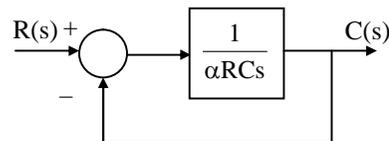
$$s^0 \quad \left| \begin{array}{l} 8 \end{array} \right.$$

There is no sign changes in the first column of RH criteria table. Therefore the

closed loop  $\frac{C(s)}{R(s)}$  is stable

**17. Ans: (a)**

**Sol:**  $\frac{V_0(s)}{V_1(s)} = \frac{1}{\alpha RCs + 1}$



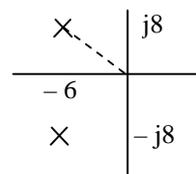
$$k_v = \lim_{s \rightarrow 0} s.G(s) = \lim_{s \rightarrow 0} s \frac{1}{\alpha RCs} = \frac{1}{\alpha RC}$$

$$e_{ss} = \frac{1}{k_v} = \alpha RC$$

**18. Ans: (d)**

**Sol:** Compare  $C(t) = ke^{-\alpha t} \sin \omega_d t u(t)$

We get  $\alpha = 6, \omega_d = 8$





The radial distance  $\omega_n = 10 \text{ rad/sec}$

$$\cos \theta = \zeta = \frac{6}{10} = 0.6$$

$$\omega_d = 8 \text{ rad/sec}$$

19. Ans: (c)

20. Ans: (c)

Sol:  $e_{ss} = \frac{A}{1+k_p}$  for step input

$$e_{ss} = \frac{A}{k_v}$$
 for ramp input

$$e_{ss} = \frac{A}{k_a}$$
 for parabolic input

Where

$$k_p = \lim_{s \rightarrow 0} s G(s), k_v = \lim_{s \rightarrow 0} s^2 G(s), k_a = \lim_{s \rightarrow 0} s^3 G(s)$$

For type 0- system,  $k_p = \text{finite} \Rightarrow e_{ss}$  is finite

For type 2-system,  $k_v = \infty \Rightarrow e_{ss} = 0$

$$k_a = \text{finite} \Rightarrow e_{ss} = \text{finite}$$

For type-1 system,  $k_p = \infty \Rightarrow e_{ss} = 0$

$\therefore$  statements 1,2 are correct

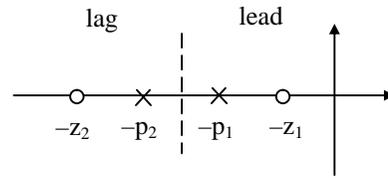
21. Ans: (d)

Sol: System is under damped when poles are on complex plane.

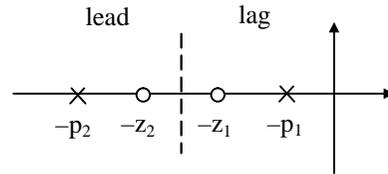
$\therefore$  For  $0.7 < k < 14$  system is under damped.

22. Ans: (a)

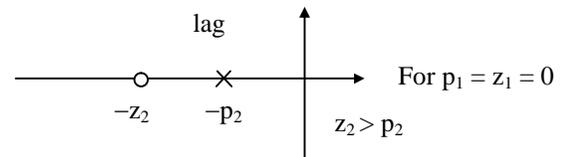
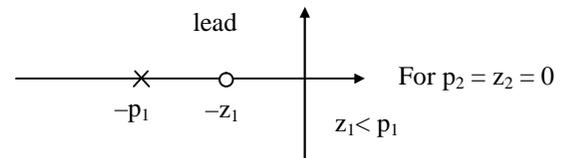
Sol:



$$z_1 < p_1 < p_2 < z_2$$



$$p_1 < z_1 < z_2 < p_2$$

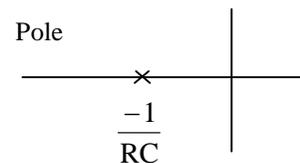


So, 1, 2, 3 correct.

23. Ans: (b)

Sol: The circuit is 1<sup>st</sup> order RC network

$$TF = \frac{1}{RCs + 1}$$



$\rightarrow$  For whatever RC value the pole location is on real axis



∴ It will never produce oscillations.

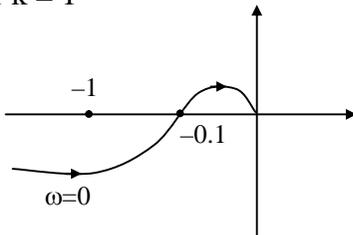
→ Since pole of the system is on real axis and the system has only one pole.

It will produce -ve phase angle for sin input, 1, 3, 4 are correct.

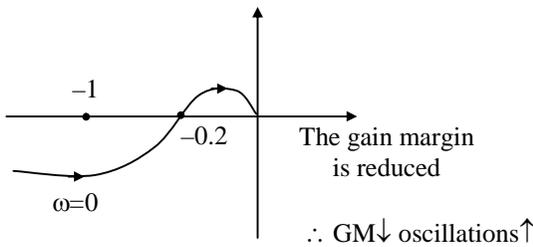
**24. Ans: (c)**

**Sol:** The plot is given for  $k = 1$

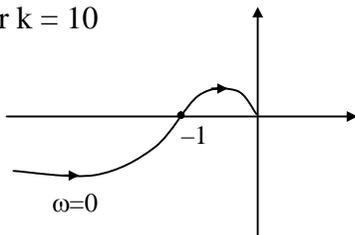
For  $k = 1$



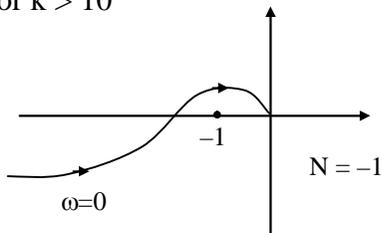
For  $k = 2$



For  $k = 10$



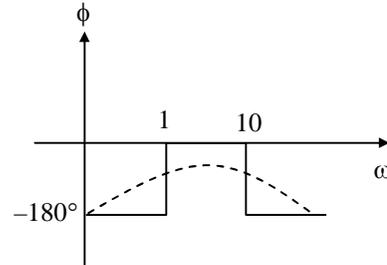
For  $k > 10$



$(-1, 0)$  is enclosed therefore system is unstable.

**25. Ans: (b)**

**Sol:**

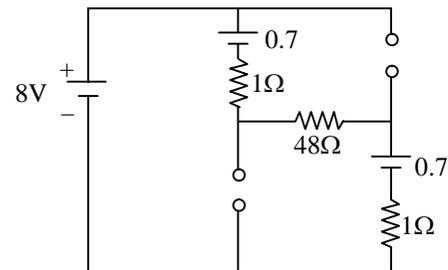


The phase plot of the system  $\omega = 10, -90^\circ$

**26. Ans: (b)**

**27. Ans: (c)**

**Sol:**



By KVL

$$8 - 0.7 - i - 48i - 0.7 - i = 0$$

$$8 - 1.4 = 50i$$

$$i = \frac{6.6}{50}$$

$$i = 0.132$$

$$i = 132 \text{ mA}$$

**28. Ans: (a)**

**29. Ans: (d)**

**Sol:**  $(\text{gain})_{\text{dB}} = 10 \log_{10}^{26/13} = 10 \log_{10}^2 = 3 \text{ dB}$



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30. Ans: (a)

Sol:  $C_1 = 1\text{nF}$ ,  $C_2 = 10\text{nF}$  &  $L = 0.1\mu\text{H}$

$$|A| \geq \frac{C_2}{C_1} = \frac{10\text{nF}}{1\text{nF}} = 10.$$

31. Ans: (d)

Sol:

The output frequency component

$$= nf_1 \pm mf_2$$

32. Ans: (d)

$$\text{Sol: } \frac{dA_f}{A_f} = \frac{dA}{A} \left( \frac{1}{1 + A\beta_f} \right)$$

$$\frac{0.1}{100} = \frac{10}{1000} \left[ \frac{1}{1 + 1000\beta_f} \right]$$

$$1 + 1000\beta_f = 10$$

$$\beta_f = \frac{9}{1000}.$$

33. Ans: (b)

Sol: gain = 30 dB

$$30\text{dB} = 10 \log_{10} \left( \frac{P_o}{P_i} \right)$$

$$\Rightarrow 3 = \log_{10} \left( \frac{P_o}{P_i} \right)$$

$$\frac{P_o}{P_i} = 10^3$$

$$P_o = 10^3 \times P_i$$

$$P_o = 10^3 \times 1 \times 10^{-6}$$

$$P_o = 10^{-3} \text{ W}, \quad P_o = 1\text{mW}$$

$$P_{o \text{ in dB}} = 10 \log_{10}^1 = 0\text{dBm}$$



34. Ans: (d)

35. Ans: (c)

Sol: Ripple factor in LC filter =  $\frac{\sqrt{2}}{3} \frac{1}{4\omega^2 CL}$

For frequency of 50Hz

ripple factor ( $\gamma$ ) =  $\frac{1.194}{LC}$

So, it remains constant.

36. Ans: (a)

37. Ans: (d)

38. Ans: (d)

Sol:  $V_T = 0.5V$

$V_{GS} = V_G - V_S = 0 - 0 = 0V$

$V_{GS} < V_T \rightarrow$  Cutoff Region

So  $I_D = 0, V_D = 6V$

39. Ans: (a)

40. Ans: (d)

Sol: For an ideal feedback circuit to have sustained oscillation the loop gain is 1. For practical feedback circuit the loop gain varies from 1.01 to 1.05 (slightly greater than one) for sustained oscillation.

41. Ans: (a)

Sol:  $A_d = 2000$

$CMRR = 1000$

$V_{non-inv} = 5.001V$

$V_{inv} = 4.999V$

Common mode gain  $A_c = \frac{A_d}{CMRR} = \frac{2000}{1000} = 2$

Differential voltage  $V_d = V_{non-inv} - V_{inv}$   
 $= 5.001 - 4.999 =$

$2 \times 10^{-3}V$

Common mode voltage

$V_c = \frac{V_{non-inv} + V_{inv}}{2} = \frac{5.001 + 4.999}{2} = 5V$

$V_0 = A_d V_d + A_c V_c$   
 $= 2000 \times 2 \times 10^{-3} + 2 \times 5$   
 $= 4 + 10$   
 $= 14V$

42. Ans: (c)

Sol: Duty cycle

$$= \frac{\text{ON Time}}{\text{ON Time} + \text{OFF Time}} = \frac{(R_A + R_B)C}{(R_A + R_B)C + R_B C}$$

$$= \frac{(R_A + R_B)}{(R_A + 2R_B)}$$

Duty cycle of the output waveform  $V_0$  not depend upon capacitor 'C'.

**GATE - 2018**

**ONLINE TEST SERIES**

**No. of Tests : 62**

All tests will be available till  
12<sup>th</sup> February 2018

**ESE - 2018 PRELIMS**

**ONLINE TEST SERIES**

**No. of Tests : 44**

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**ISRO - 2017**

**ONLINE TEST SERIES**

**No. of Tests : 15**

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25<sup>th</sup> December 2017

★ HIGHLIGHTS ★

- Detailed solutions are available.
- **All India rank** will be given for each test.
- Comparison with all India toppers of **ACE** students.

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43. Ans: (c)

44. Ans: (c)

45. Ans: (c)

**Sol:** For the given input voltages

D1 will be ON & D2 will be OFF

⇒ Voltage at 'P' will be 2V

$$\therefore I = \frac{5V - 2V}{1K} = 3mA$$

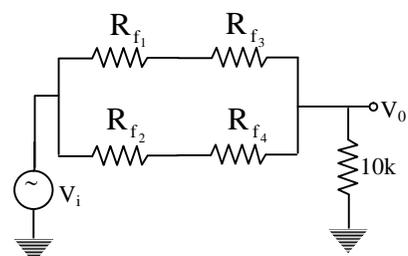
46. Ans: (d)

47. Ans: (b)

**Sol: Step 1:** Forward dynamic resistance of the diodes,

$$R_f = \frac{V_T}{I_D} = \frac{0.025V}{\frac{1mA}{2}} = 50\Omega$$

**Step 2:** Equivalent circuit of figure





Note:  $R_{f_1} = R_{f_2} = R_{f_3} = R_{f_4} = R_f$   
( $\therefore$  All the diodes are identical)

$$V_0 = \frac{10K V_i}{10K + [2R_f \parallel 2R_f]}$$

$$\frac{V_0}{V_i} = \frac{10K}{10K + [100\Omega \parallel 100\Omega]}$$

$$\therefore \frac{V_0}{V_i} = 0.995$$

48. Ans: (c)

Sol: We have, line regulation,  $\eta_i = \frac{\Delta V_0}{\Delta V_i}$

$$= \frac{r_z}{r_z + R_s}$$

$$= \frac{10}{10 + 80}$$

$$= \frac{1}{9}$$

$$\Rightarrow \frac{\Delta V_0}{\Delta V_i} = \frac{1}{9}$$

$$\therefore \Delta V_0 = \frac{1}{9} \times \Delta V_i = \frac{1}{9} \times 0.9V = 100mV$$

49. Ans: (a)

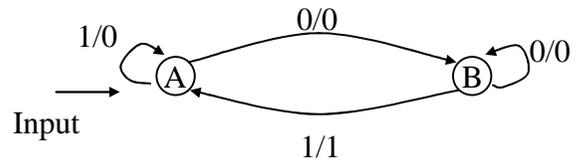
Sol: Binary zero has unique representation in 2'S complement representation. So this representation is widely used.

50. Ans: (b)

51. Ans: (c)

52. Ans: (c)

Sol: The given state diagram detects 01,001,001,00001,.....



53. Ans: (a)

Sol: A 01

A 00, (Cy = 0, AC = 0)

Loop: A FF (bit carry flag is not affected JNC loop is failed)

Hence HLT is executed

54. Ans: (d)

55. Ans: (a)

56. Ans: (c)

57. Ans: (b)

Sol: (a)& (c) are not valid instructions.

SBI 98H  $\Rightarrow$  subtract immediate with borrow

SUI 98H  $\Rightarrow$  subtract immediate (no borrow)

58. Ans: (a)

Sol: XTHL exchanges the contents of L register with the contents of memory location specified by the stack, pointer the contents of the H register are exchanged with the contents of stack pointer +1.



59. Ans: (a)

60. Ans: (a)

61. Ans: (d)

**Sol:** All are the properties of EEPROM. EEPROM'S are fabricated using NMOS /CMOS, where as PROMS and ROMS use bipolar TTL. Hence EEPROM'S have longer delays.

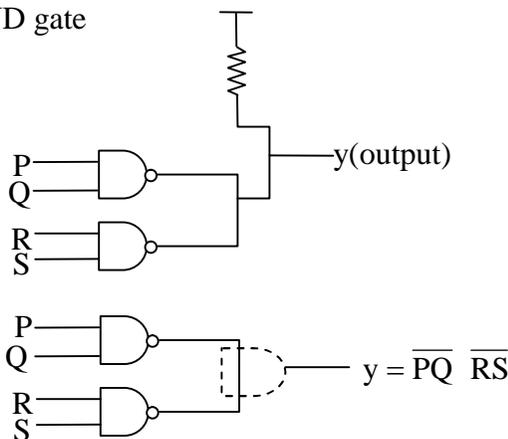
62. Ans:(d)

**Sol:**

(i)	(ii) HL ← 5000H	(iii) A ← 6AH
A ← 96H	M ← 96H	A ← 95H
96H → (5000H)	M ⇒ contents of HL	A ← 96 → (5000)

63. Ans:(a)

**Sol:** Whenever open collector (TTC) configuration then wired connection is AND gate



64. Ans:(c)

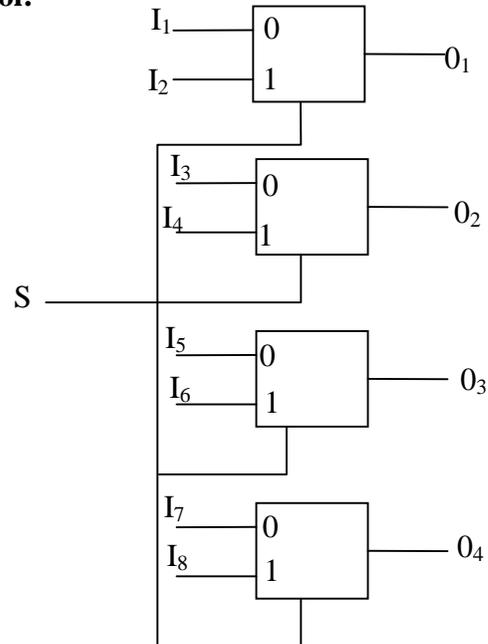
**Sol:** 64K ⇒  $2^{16} = 2^8 \times 2^8$  (Coincident decoding)

$$= 256 \times 256$$

Each decoder is  $8 \times 256$  side

65. Ans: (a)

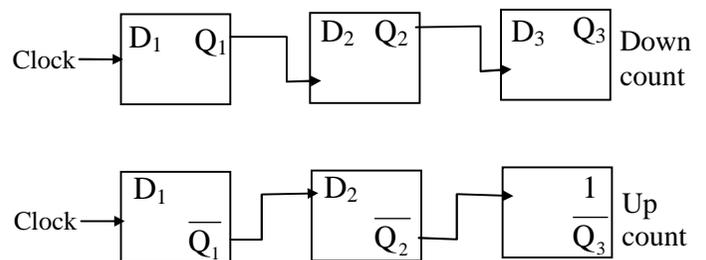
**Sol:**



Total 9 input 4 outputs so ROM side  $= 2^9 \times 4$   
( $2^{\text{no of inputs}} \times \text{no of outputs}$ )

66. Ans: (c)

**Sol:** Both statements are correct

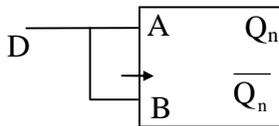
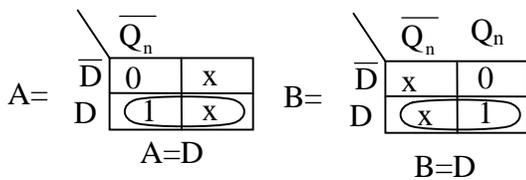




67. Ans: (a)

Sol:

D	Q <sub>m</sub>	Q <sub>n</sub>	A	B
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	X	1

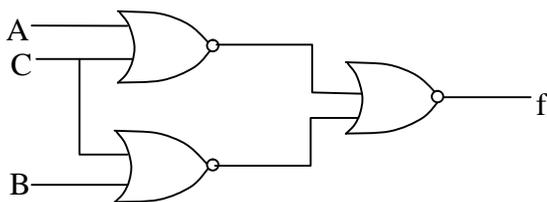


68. Ans: (b)

Sol:  $f = AB + C$

$$F = (A + C) B + C$$

To implement using NOR gates, go for POS form.



69. Ans: (a)

Sol: To check commutative  $\Rightarrow x \oplus y = y \oplus x$

$$\text{L.H.S } x \oplus y = x^2 + y^2 \rightarrow (1)$$

$$\text{R.H.S } y \oplus x = y^2 + x^2 \rightarrow (2)$$

$$(1) = (2)$$

To check associative

$$\Rightarrow (x \oplus y) \oplus z = x \oplus (y \oplus z)$$

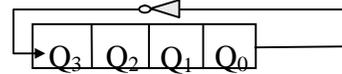
$$\begin{aligned} \text{L.H.S } (x \oplus (y \oplus z)) &= (x^2 + y^2) \oplus z \\ &= (x^2 + y^2) + z^2 \rightarrow (3) \end{aligned}$$

$$\begin{aligned} \text{R.H.S } x \oplus (y \oplus z) &= x \oplus (y^2 + z^2) \\ &= x^2 + (y^2 + z^2)^2 \rightarrow (4) \end{aligned}$$

$$(3) \neq (4)$$

70. Ans: (d)

Sol:



Clock	0	0	0	0
1	1	0	0	0 (8)
2	1	1	0	0 (12)
3	1	1	1	0 (14)
4	1	1	1	1 (15)
5	0	1	1	1 (7)
6	0	0	1	1 (3)
7	0	0	0	1 (1)
8	0	0	0	0 (0)

71. Ans: (b)

Sol:  $\rightarrow$  Its noise immunity and power dissipation are worst of all logic families

$\rightarrow$  The outputs provide "OR" and "NOR" families

$\rightarrow$  Because of high speed, external wires act like transmission lines



72. Ans: (a)

Sol: Slew Rate (SR) =  $\left. \frac{dV_0}{dt} \right|_{\max}$

In ideal Op – Amp Slew Rate is Very high

73. Ans: (a)

74. Ans: (a)

75. Ans: (c)